IN THE SPECIFICATION

Please replace the paragraph at page 2, lines 6-24, with the following rewritten paragraph:

For writing logic "1" data in the FBC memory, impact ionization near the drain of a memory cell is utilized. More specifically, ~~while~~ giving appropriate bias conditions for permitting flow of a significant channel current in the memory cell~~, cause~~ causes majority carriers that are produced by impact ionization to be stored in the floating body. Writing logic "0" data is performed by setting a PN junction between the drain and the body in a forward bias state to thereby release the body's majority carriers toward the drain side.

Please replace the paragraph at page 7, lines 5-14, with the following rewritten paragraph:

For writing logic "0" data, a forward bias current flowable between the drain and the floating body of a memory cell is utilized. For example as shown in Fig. 13, ~~apply~~ a negative voltage of -1V is applied to a presently selected bit line BL while simultaneously giving a 1.5V voltage to a selected word line WL. With such voltage application, the holes that are stored in the floating body of a selected memory cell are drawn out from the body toward the bitline BL through the forward-biased PN junction. The resulting state with no excess holes in the body is the data "0" storage state.

Please replace the paragraph at page 7 lines 15-33, with the following rewritten paragraph:

After completion of data write, the stored data is retained by applying to the wordline WL a holding voltage with the negative polarity, for example, -1.5V. Data read is done by potentially biasing the memory cell in its turn-on state which precludes occurrence of impact

ionization and then detecting a cell current flowing therein. For example as shown in Fig. 14, ~~apply~~ a voltage of 1.5V is applied to the selected word line WL and ~~apply~~ a 0.2V voltage is applied to the selected bit line BL. Whereby, the memory cell of interest is set in an on-state within a triode operation region (linear region). The floating body's hole storage state, which differs depending upon whether data "0" or "1" is stored therein, becomes a difference in back-bias, which in turn leads to a difference in threshold voltage of the memory cell. Accordingly, the memory cell is different in current characteristics curve in a way depending on whether the stored data is a logic "0" or "1" as shown in Fig. 15. Thus it is possible to determine or identify whether the stored data is a logic "0" or "1" by detecting a cell current difference ΔIds between the both.

Please replace the paragraph at page 10, lines 18-24, with the following rewritten paragraph:

Therefore, a NMOS transistor MN2 disposed between the node N11 of the ~~dada~~ data latch 43 and the write data transferring line 46 serves as a transfer circuit 104c for transferring the write data to the cell array 101. In this embodiment, this transfer circuit 104c serves for also writing back the read data in the ~~dada~~ data latch 43 into the selected cell of the cell array.

Please replace the paragraph at page 11, lines 13-22, with the following rewritten paragraph:

The dummy clamp circuit 44a is configured ~~as similar~~ similarly to the clamp circuit 44 to be used for clamping voltages of the reference bit lines RBL1, RBL0 in the read mode. To the reference node N2, two current source load PMOS transistors MP2a, MP2b, which are diode-connected, are connected. Each of these load transistors MP2a, MP2b has the same

size and current drivability as the load PMOS transistor MP1. In place of these two load PMOS transistors MP2a, MP2b, one load PMOS transistor, current drivability of which is twice as high as that of the load transistor MP1 at the sense node N1, may be used.

Please replace the paragraph at page 15, lines 7-21, with the following rewritten paragraph:

On the other hand, t_D is a time ~~in which~~ taken to reach a data discrimination impossible state due to that the threshold of "0" data ~~changes~~ changing toward that of "1" data by continuing the read state. In other words, t_D is a retention time in which it is possible to continue the data read state without data destruction. The situation of what degree shift of "0" data threshold causes data discrimination to be impossible is determined by the sense amplifier circuit. Suppose that such threshold shift is $\Delta Vth0$. The time t_D taken for the threshold voltage of "0" data to be ~~sifted~~ shifted by $\Delta Vth0$ is determined by the amount of holes generated by impact ionization. The impact ionization becomes remarkable in a state that the cell transistor is biased in the current saturation region. In the current saturation region, as the bit line voltage is higher, the amount of generated holes ~~becomes more~~ increases.

Please replace the paragraph at page 15, line 32 to page 16, line 5, with the following rewritten paragraph:

Referring to the sense amplifier circuit shown in Fig. 1, data read operation will next be described ~~bellow~~ below. Fig. 4 shows waveforms of main signals in the read operation. The read operation is, as above-described, performed by two steps, STEP1 and STEP2. In the first step STEP1, set the sense amplifier activating signals SAEN and SAENn at "H" and "L", respectively, further set the latch signal LTC at "H", and sense amplifier circuit 103 is

activated. A cell data selected by a word line WL and a bit line BL is transferred to the sense node N1 via bit line selector 102 and clamp circuit 44.

Please replace the paragraph at page 17, line 28 to page 18, line 2, with the following rewritten paragraph:

As described above, preparing such a function that data "1" and "0" are simultaneously written into the reference cells RMC1 and RMC0, it also becomes possible to simultaneously refresh the reference cells RMC1 and RMC0. Further, it is also possible to refresh the reference cells RMC1 and RMC0 simultaneously with the normal ~~dell~~ cell MC. As a result, it is ~~able~~ possible to shorten the time period necessary for data refreshing. The scheme of shortening the refresh time by use of the switch circuit 102a is useful even if the scheme of shortening the read time by the above-described data read with two steps is not used.

Please replace the paragraph at page 18, lines 18-25, with the following rewritten paragraph:

As above-described, in this embodiment, a read sequence is used to include a read step STEP1, in which the bit line voltage is set higher than that in the prior art, and a write back step STEP2 for writing back the read data right after it ~~having~~ has been read out. As a result, it is possible to shorten the read time of the FBC memory. In addition, as a result of using ~~that~~ a high bit line voltage ~~is used~~, sensibility of the FBC memory may be improved.

Please replace the paragraph at page 19, lines 8-16, with the following rewritten paragraph:

Fig. 3 shows another example of the sense amplifier circuit 103. In the sense amplifier circuits shown in Fig. 1 and 2, the transfer circuit 104c is used for not only normal ~~dada~~ data write operations but also write back operations in the read cycles. The write back is done also when "1" data is read out. However, "1" data write back uselessly performs bit line charge/discharge. In view of reducing power consumption, it can be said that "1" data write back is not desirable rather than it is unnecessary as described above.